North East University Bangladesh

Department of Computer Science and Engineering

**Lab Report**

**Experiment Name:** Diode Circuit Analysis

**Experiment No:** 02

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# Objective

The objective of this experiment is to analyse simple diode circuits and to build logic circuits using diodes and resistors.

# Theory

Theory needed for this lab should be read from lecture 3 of theory course.

## Apparatus Needed

* + Trainer Board (Bread board)
  + Diodes
  + Resistor
  + DC Voltmeter
  + DC Ammeter
  + DC power supply
  + Function Generator
  + Oscilloscope
  + Connecting wires

## **Circuits**

For analysis of diode circuit. Here, I have shown three figures (1,2,3) circuit for diode analysis.

Diagram, schematic

Description automatically generated

Figure 1 Circuit for diode analysis

Diagram, schematic

Description automatically generated

Figure 2 Positive Logic OR Gate

Diagram, schematic

Description automatically generated

Figure 3 Positive Logic AND Gate

## Procedure

1. Analytically find 𝐼𝐷, 𝑉𝐷2, 𝑎𝑛𝑑 𝑉0 for the circuit in figure 1 and record the result in table 1.
2. Implement the circuit in figure 1.
3. Find 𝐼𝐷, 𝑉𝐷2, 𝑎𝑛𝑑 𝑉0 from the circuit and record the result in table 1.5V
4. Implement the circuit in figure 2 and apply inputs according to the table 2 and note the output voltages in table 2 to check if OR gate is properly implemented or not.
5. Implement the circuit in figure 3 and apply inputs according to the table 3 and note the output voltages in table 3 to check if AND gate is properly implemented or not.

Table 1 Data for circuit 1

|  |  |  |
| --- | --- | --- |
| **Measurement** | **Theoretical value (Step 1)** | **Practical value (Step 2)** |
| ID |  |  |
| 𝑉𝐷2 |  |  |
| V0 |  |  |

Table 2 Data for circuit 2

|  |  |  |  |
| --- | --- | --- | --- |
| Input 1 Voltage | Input 2 Voltage | Output Voltage | Output logic level |
| 0 V | 0 V |  |  |
| 0 V | 5 V |  |  |
| 5 V | 0 V |  |  |
| 5 V | 5 V |  |  |

Table 3 Data for circuit 3

|  |  |  |  |
| --- | --- | --- | --- |
| Input 1 Voltage | Input 2 Voltage | Output Voltage | Output logic level |
| 0 V | 0 V |  |  |
| 0 V | 5 V |  |  |
| 5 V | 0 V |  |  |
| 5 V | 5 V |  |  |

# Report

1. Carefully Fill all the data for table 1, 2, 3.

2. Comment on the learnings from this LAB.